FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICE

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(USE SEVERAL SHEETS IF NECESSARY)

ATTY. DOCKET NO.	APPLICATION NO.
ARC.005A	09/523,877
APPLICANT: Peter Warnes, et al.	
FILING DATE: March 13, 2000	GROUP: 2784

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
DJH	1	5,724,566	03/03/98	Swoboda			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
DJH	2	0355069 A	Feb. 1990	EPO				
DJH	3	0476628 A	March 1992	EPO				

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
DJH	4	Piyush Patel, et al., "Architectural Features of the i860™ - Microprocessor RISC Core and On-Chip Caches," Proceedings of the International Conference on Computer Design: VLSI In Computers and Processors (1989), pp. 385-390

EXAMINER David J. Huisman	DATE CONSIDERED 12-9-02

*EXAMINER: INITIAL IF CITATION CONSIDERED, WHETHER OR NOT CITATION IS IN CONFORMANCE WITH MPEP 609; DRAW LINE THROUGH CITATION IF NOT IN CONFORMANCE AND NOT CONSIDERED, INCLUDE COPY OF THIS FORM WITH NEXT COMMUNICATION TO APPLICANT.

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DJH	5	5,491,640	02/13/96	Sharma, et al.			
DJH	6	5,493,508	02/20/96	Dangelo, et al.			
DJH	7	5,502,661	03/26/96	Wolfgang Glunz			
DJH	8	5,537,580	07/16/96	~~Giomi, et al.~~ Fiami et al			
DJH	9	5,544,067	08/06/96	Rostoker, et al.			
DJH	10	5,555,201	09/10/96	Dangelo, et al.			
DJH	11	5,801,958	09/01/98	Dangelo, et al.			
DJH	12	5,812,416	09/22/98	Gupte, et al.			
DJH	13	5,841,663	11/24/98	Sharma, et al.			
DJH	14	5,854,930	12/29/98	McLain, et al.			
DJH	15	5,898,595	04/27/99	Bair, et al.			
DJH	16	6,026,219	02/15/00	Miller, et al.			
DJH	17	6,110,223	08/29/00	Southgate, et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
DJH	18	WO 97 13209 A	April 1997	WIPO				

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
DJH	19	Elms, A., "Tuning a Customisable RISC Core for DSP," Electronic Product Design, Sept. 1997, Vol. 18, No. 9, pages 19-20, 22, XP000909039
DJH	20	Berekovic, Mladen, et al., "A Core Generator for Fully Synthesizable and Highly Parameterizable RISC-Cores for System-On-Chip Designs, 1998 IEEE Workshop on Signal Processing Systems, Pages 561-568, XP-002137267
DJH	21	Yang, Jin-Hyuk, et al., "MetaC ore: A Configurable & Instruction-Level Extensible DSP Core, " Proceedings of the ASP-DAC '98 Asian and South Pacific Design Automation Conference 1998, pages 325-326, XP -002137268

EXAMINER INITIAL		OTHER DOCUMENTS (INCLUDING AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.)
DJH	22	Application Serial No. 09/418,663 entitled "Method and Apparatus for Managing the Configuration and Functionality of a Semiconductor Design," filed October 14, 1999 – Attorney Docket No. ARC.001A
DJH	23	Application Serial No. 09/523,871 entitled "Method and Apparatus for Jump Control in a Pipelined Processor," filed March 13, 2000 – Attorney Docket No. ARC.006A
DJH	24	Application Serial No. 09/524,179 entitled "Method and Apparatus for Processor Pipeline Segmentation and Re-Assembly," filed March 13, 2000 – Attorney Docket No. ARC.007A
DJH	25	Application Serial No. 09/524,178 entitled "Method and Apparatus for Loose Register Encoding Within a Pipelined Processor," filed March 13, 2000 – Attorney Docket No. ARC.008A

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